Amendments to the Claims:

1 (currently amended):   A computer readable medium
encoded with instructions for executing [[the]] steps of:
    performing a cell placement for an integrated circuit
design;
    receiving information representative of [[about]] a
driving cell and ~~from a layout tool, receiving information
about~~ an interconnect in the integrated circuit design ~~from a
layout tool~~;
    retrieving a previously defined critical net length
associated with the driving cell and the interconnect from
~~determining buffer cell information based upon information
about the driving cell and the interconnect by accessing~~ a
~~previously defined~~ library lookup table;
    comparing a net length of the interconnect with the
previously defined critical net length; and
    if the interconnect length exceeds the previously defined
critical net length, then:
        selecting a buffer cell from the library lookup
table to meet a given performance constraint for the
interconnect; and
        generating as output information representative of
the buffer cell for inserting the buffer cell in the
interconnect ~~relaying the buffer cell information~~ from the
library look up table ~~to the layout tool~~.

    2 (currently amended):   The computer readable medium
of claim 1[[,]] wherein the step of receiving information
representative of [[about]] an interconnect includes receiving
a net length of the interconnect.

3 (currently amended): The computer readable medium of claim 1[[,]] wherein the step of receiving information <u>representative of</u> [[about]] an interconnect includes receiving hanging capacitance.

4 (currently amended): The computer readable medium of claim 3[[,]] wherein <u>the</u> [[said]] hanging capacitance represents [[the]] capacitance of branches emanating from <u>the</u> [[said]] interconnect[[,]] ~~said interconnect electrically coupling said driving cell with a receiving cell~~.

5 (currently amended): The computer readable medium of claim 1[[,]] wherein the step of receiving information <u>representative of</u> [[about]] a driving cell includes receiving input ramp time.

6 (canceled)

7 (currently amended): The computer readable medium of claim <u>1</u> [[5,]] wherein <u>the step of selecting a</u> ~~said requesting said~~ buffer cell ~~information~~ further comprises:
    <u>determining</u> ~~requesting~~ at least one buffer cell location;
    <u>determining</u> ~~requesting~~ at least one type of buffer cell; and
    <u>determining</u> ~~requesting~~ a quantity of the <u>at least one</u> type of buffer cell.

8 (currently amended): The computer readable medium of claim <u>7</u> [[5,]] wherein <u>determining</u> ~~said requesting~~ at least one type of buffer cell includes <u>selecting</u> ~~requesting~~ at least one type of buffer cell as a function of the net length and <u>an</u> [[a]] input ramp time.

9 (currently amended): The computer readable medium of claim 7 [[6,]] wherein the step of generating as output information representative of the selected buffer cell for inserting the selected buffer cell in the interconnect further comprises comprising. relaying to a [[said]] layout tool the [[said]] at least one buffer cell location, the [[said]] at least one type of buffer cell, and the [[said]] quantity of the at least one type of buffer cell.

10 (currently amended): A method comprising steps of:

performing a cell placement for an integrated circuit design generating a library lookup table;

receiving information representative of [[about]] a driving cell and an interconnect in the integrated circuit design [[from a layout tool]];

retrieving a previously defined critical net length associated with the driving cell and the interconnect from a determining buffer cell information by accessing the library lookup table;

comparing a net length of the interconnect with the previously defined critical net length; and

if the interconnect length exceeds the previously defined critical net length, then:

selecting a buffer cell from the library lookup table to meet a given performance constraint for the interconnect; and

generating as output information representative of the buffer cell for inserting the buffer cell in the interconnect relaying the buffer cell information from the library look up table to the layout tool.

        11 (currently amended)   The method of claim 10
further comprising ~~, wherein said~~ generating the [[a]] library
lookup table by ~~includes~~ empirically establishing the ~~said~~
~~buffer cell~~ information representative of the buffer cell.

        12 (currently amended):   The method of claim 10
[[,]] wherein the step of [[said]] receiving information about
the [[said]] interconnect includes receiving a net length of
the interconnect.

        13 (currently amended):   The method of claim 10
[[,]] wherein the step of [[said]] receiving information about
the [[said]] interconnect includes receiving hanging
capacitance of the interconnect from the [[said]] layout
tool.[[.]]

        14 (currently amended):   The method of claim 13[[,]]
wherein the [[said]] hanging capacitance represents [[the]]
capacitance of branches emanating from the [[said]]
interconnect[[,]] ~~said interconnect electrically coupling said~~
~~driving cell with a receiving cell~~.

        15 (currently amended):   The method of claim 10
wherein the step of selecting a ~~said determining~~ buffer cell
~~information~~ further comprises:
        determining at least one buffer cell location;
        determining a quantity of buffer cells; and
        determining at least one type of buffer cell.

        16 (currently amended):   A buffer insertion system
comprising:
        a library lookup table;

receiving means for obtaining information <u>representative</u>
<u>of</u> [[about]] a driving cell and an interconnect [[from a
layout tool]];

buffer determination means for <u>selecting</u> [[obtaining]] at
least one type of buffer cell, a quantity of buffer cells, and
a distance between buffer cells from the library lookup table
based upon <u>a</u> [[the]] net length <u>of the interconnect</u> and the
~~driving cell~~ information <u>representative of the driving cell</u>;
<u>and</u>

sending means for delivering the <u>at least one</u> type of
buffer cell, <u>the</u> [[a]] quantity of buffer cells, and <u>the</u> [[a]]
distance between buffer cells to <u>a</u> [[the]] layout tool.

17 (currently amended): The buffer insertion system
of claim <u>16</u> [[15,]] wherein <u>the</u> [[said]] receiving means for
obtaining information includes means for receiving a net
length <u>of the interconnect</u>.

18 (currently amended): The buffer insertion system
of claim 16, wherein <u>the</u> [[said]] buffer determination means
includes:

means for selecting a predetermined <u>critical</u> net length
from the library lookup table based upon <u>the</u> [[said]] net
length <u>of the interconnect</u> and <u>the</u> [[said driving cell]]
information <u>representative of the driving cell</u>; and

means for comparing <u>the</u> [[said]] <u>critical</u> net length <u>of</u>
<u>the interconnect</u> with <u>the</u> [[said]] predetermined net length.

19 (canceled)

20 (new): A buffer insertion system comprising:

a design automation tool for performing a cell placement for an integrated circuit design;

a design automation tool interface for receiving information representative of a driving cell and an interconnect in the integrated circuit design from the design automation tool;

a library lookup table for identifying a previously defined critical net length associated with the driving cell and the interconnect; and

a length comparator for retrieving the previously defined critical net length from the library lookup table, for comparing a net length of the interconnect with the previously defined critical net length, and for selecting a buffer cell for insertion in the interconnect to meet a given performance constraint.